CLAIMS

What is claimed is:

1. An integrated circuit comprising:

a first bus;

a second bus;

a third bus;

a shunting circuit including a plurality of transistors in a stacked configuration, the shunting circuit having a plurality of control terminals, a first current terminal coupled to the first bus, and a second current terminal coupled to the second bus, wherein the shunting circuit is made conductive to provide a discharge path from the first bus to the second bus for current from an electrostatic discharge (ESD) event;

a trigger circuit having a first output coupled to a first control terminal of the plurality of control terminals of the shunting circuit to provide a first control signal and having a second output coupled to a second control terminal of the plurality of control terminals of shunting circuit to provide a second control signal, the trigger circuit is coupled to the third bus;

a pad, the pad coupled to the first bus, the second bus, and the third bus.

2. The integrated circuit of claim 1 further comprising:

a pull-up device, the pad coupled to the third bus via the pull-up device.

3. The integrated circuit of claim 2 wherein the pull-up device includes a diode.

4. The integrated circuit of claim 1 wherein during a detection of an ESD event, the first output and the second output are pulled to substantially a voltage of the third bus to make conductive the shunting circuit to discharge current of the ESD event from the first bus to the second bus.

5. The integrated circuit of claim 1 wherein the trigger circuit further comprises a first switch and a second switch, wherein during the detection of an ESD event, the first switch and the second switch are made conductive to provide a current path between the third bus and the first output and between the third bus and the second output.

6. The integrated circuit of claim 1 wherein during a normal operation of the integrated circuit, the first output is pulled substantially to a voltage of a fourth bus, and the second output is pulled substantially to a voltage of the second bus, wherein the voltage of the fourth bus is different than the voltage of the second bus.

7. The integrated circuit of claim 6 wherein:

the plurality of transistors are of a process technology having an associated maximum voltage, the first output being pulled substantially to the voltage of the fourth bus and the second output being pulled substantially to the voltage of the second bus places the transistors of the plurality in a state such that a voltage drop

across each transistor of the plurality is less than the maximum voltage.

8. The integrated circuit of claim 1 wherein during a normal operation of the integrated circuit, the first output is at a first voltage, and the second output is a second voltage, the first voltage is different from the second voltage.

9. The integrated circuit of claim 1 wherein during a normal operation of the integrated circuit, the trigger circuit provides a current path between a fourth bus and the first output and provides a second current path between the second bus and the second output.

10. The integrated circuit of claim 1 wherein:

the trigger circuit includes an internal node;

during a normal operation, the internal node is pulled substantially to a voltage of a fourth bus;

during a normal operation, the fourth bus is at a power supply voltage;

during an ESD event, the internal node is pulled substantially to a voltage of the third bus.

11. The integrated circuit of claim 10 wherein:

the trigger circuit includes a pull-up circuit, wherein the pull-up circuit includes a capacitive pull-up device and/or a conductive pull-up device, wherein the internal node is coupled to the third bus via the capacitive pull-up device and/or the conductive pull-up device during an ESD event.

12. The integrated circuit of claim 11 wherein the conductive pull-up device is controlled by an output of an RC circuit.

13. The integrated circuit of claim 10, wherein the trigger circuit includes a detection circuit coupled to the internal node, the detection circuit detects an ESD event via the internal node.

14. The integrated circuit of claim 1 wherein the trigger circuit includes a slew rate detection circuit for detecting an ESD event.

15. The integrated circuit of claim 1 wherein the shunting circuit includes an intermediate current terminal coupled to a fourth bus.

16. The integrated circuit of claim 1 wherein the transistors of the plurality are MOSFETS.

17. The integrated circuit of claim 1 further comprising:

a second shunting circuit including a plurality of transistors in a stacked configuration, the second shunting circuit having a first current terminal coupled to the first bus and a second current terminal coupled to the second bus, wherein the second shunting circuit is made conductive to provide a discharge path from the first bus to the second bus for current from an ESD event;

wherein the first output is coupled to a first control terminal of the second shunting circuit to provide the first control signal and the second

output is coupled to the second control terminal of the second shunting circuit to provide the second control signal.

18. The integrated circuit of claim 1 further comprising:

a fourth bus, the first control terminal coupled to the first output via the fourth bus;

a fifth bus, the second control terminal coupled to the second output via the fifth bus.

19. The integrated circuit of claim 18 wherein:

the pad and the shunting circuit are located in an I/O cell;

the I/O cell includes a diode;

the pad is coupled to the third bus via the diode.

20. The integrated circuit of claim 18 wherein:

the shunting circuit is located in an I/O cell; and

the trigger circuit is located outside of the I/O cell.

21. The integrated circuit of claim 18 further comprising:

a plurality of shunting circuits coupled to a single trigger circuit.

22. The integrated circuit of claim 1 further comprising:

a second pad, the second pad is coupled to the first bus, the second bus, and the third bus.

23. The integrated circuit of claim 1 wherein:
the integrated circuit operates at a first supply voltage,
the pad is coupled to receive external signals at a second voltage, the second voltage being higher than the first voltage.

24. The integrated circuit of claim 1 further comprising:
the trigger circuit is implemented with a plurality of transistors of a process technology having an associated maximum voltage, wherein during normal operation, the boost bus is at a higher voltage than the maximum voltage.

25. The integrated circuit of claim 1 wherein during an ESD event, the third bus is at a higher voltage than the first bus.

26. A trigger circuit for an ESD protection circuit, the trigger circuit comprising:
a detection circuit for detecting an ESD event;
an internal node, the detection circuit detecting an ESD event via the internal node;
wherein during normal operation, the internal node is coupled to a first bus;
wherein during an ESD event, the internal node is coupled to a second bus via a pull-up circuit.

27. The trigger circuit of claim 26 wherein during normal operation, the second bus is at a greater voltage than the first bus.

28. The trigger circuit of claim 27 wherein the pull-up circuit includes a capacitive pull-up device and/or a conductive pull-up device, wherein the internal node is coupled to the third bus via the capacitive pull-up device and/or the conductive pull-up device during an ESD event.

29. The trigger circuit of claim 26 further comprising:

a first output;

a second output;

during an ESD event, the trigger circuit providing at the first output and the second output, a first voltage;

wherein during normal operation, the trigger circuit providing a second voltage at the first output and a third voltage at the second output, the second voltage being different than the first voltage.

30. A method of operating an (electrostatic discharge) ESD circuit, the method comprising:

providing, in response to detecting an ESD event, a first control signal and a second control signal at a voltage substantially equal to a voltage of a first bus of an integrated circuit to a first control terminal and a second control terminal, respectively, of a shunting device, wherein the first control signal and the second control signal being at the voltage makes conductive the shunting circuit to discharge current of the ESD event from a second bus to a third bus;

providing, during a normal operation of an integrated circuit, the first control signal at a second voltage and the second control signal at a third voltage, wherein the second voltage is less than third voltage.

31. The method of claim 30 wherein the second voltage and the third voltage are at voltage levels so as to minimize leakage current through the shunting circuit.